**National University of Computer and Emerging Sciences**

**(Islamabad Campus)**

Department of Computer Science

**Signature of Invigilator: \_\_\_\_\_\_\_\_\_\_\_\_\_\_ Serial No:\_\_\_\_\_\_\_\_\_**

EE-105 Computer Logic Design

Final Examination (Spring 2013)

**Instructor(s):**

Dr Ayub Alvi, Ms Mehreen Alam, Mr Adnan Saeed

Monday May 27, 2013

**Total Marks: 100 Time Allowed: 3 hour**

Please read the instructions carefully:

1. Understanding the question paper is also part of the exam, so do not ask any clarification.
2. Solve questions in the space provided, or if you need more space write on the back side of the paper and clearly mark question and part number etc..
3. It is a CLOSED book/notes exam.
4. Calculators are NOT allowed.
5. Write your name and roll number on each page.
6. The question paper is printed on both sides of the pages.
7. Use permanent ink pens only. Any part done using soft pencil will not be marked and cannot be claimed for rechecking.

**Roll No: \_\_\_\_\_\_\_\_\_ Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Signature\_\_\_\_\_\_\_\_\_\_\_\_ Sec: \_\_\_**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Question | 1 | 2 | 3 | 4 | Total |
| Total Marks | 10 | 10 | 10 | 10 | 40 |
| Marks Obtained |  |  |  |  |  |

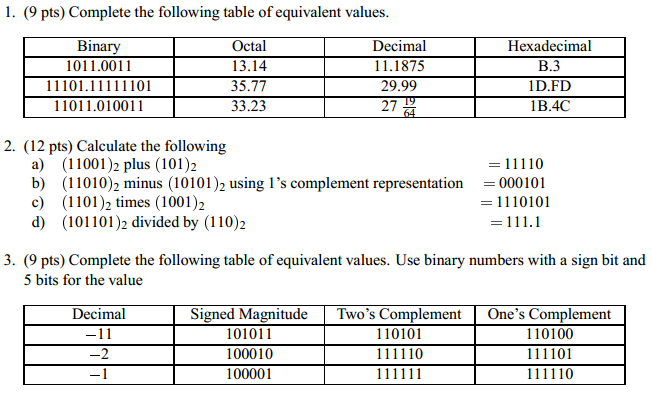
Vetted By: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Vetter Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

**Question # 1[10 = 1, 1, 1, 1, 2, 2, 2]**

1. Draw the logic diagram using minimal number of NOR gates (2,3 and 4 input gates are allowed) to implement the following function.

F(A,B,C,D) = [ ( (A’+B’+C) D ) xor (AB)’ ] + (C’ D)

1. Indicate how nand gate can be used to implement
2. And inverter
3. An and gate
4. An or gate



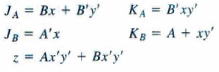
**Question # 2[10 = 5, 5] chapter 5**

Question:

Give the characteristic and excitation table for D,T and JK FF.

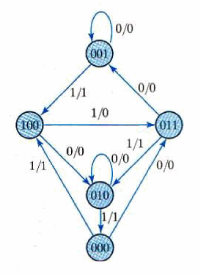
Question:

A sequential circuit has two JK flip flops A and B, two inputs x and y, and one output z. The FF input equations and circuit output equations are:



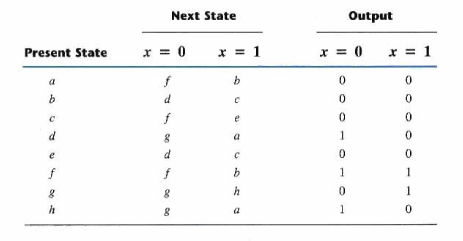
1. Draw the logic diagram of the ciruit.
2. Tabulate the state table.
3. Derive the state equations for A and B.

Question:

the sequential circuit has three FF, one input and one output. The state diagram is shown as above. The circuit is to be designed by treating the unused states as don’t care conditions. Analyse the circuit obtained from the logic design to determine the effect of unused states.

1. Use D ff for the design
2. Use J/K ff for the design

Question: Reduce the state table in the following state table, and tabulate the reduced state table.



**Question # 3[10 = 3, 3, 4] chapter 6**

Design a counter with the following repeat sequence: 0,1,2,3,4,5,6 using J/K flip flops.

Question3:

1. Design a synchronous counter with T-flip flops that goes though the following binary repeated sequence: 0,2,3,4,5,6. Take the unused states as don’t cares.
2. Show that when binary states 001 and 111 are taken as don’t care conditions, the counter may not operate properly.
3. Modify the state diagram to ensure counter operates properly even though it has entered an unused state accidently.

Draw (do not design) and label the logic diagram for a 3-bit ripple counter implemented with T-flip flops.

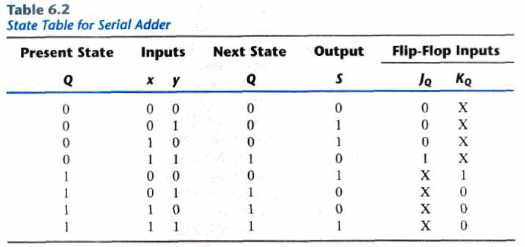
Question1:

1. Design a 3-bit synchronous counter with D-flip flops.
2. Design a 3-bit synchronous counter with J/K-flip flops.
3. Design a 2-bit synchronous counter with T-flip flops.

**Question:**

**State table for serial addition using serial register is given as follows using T FF.**

1. **Write corresponding equations.**
2. **Draw the resultant sequential circuit for it.**

****

**Question # 4[10 = 6, 2, 2] chapter 7**

Hamming Code – ROM/RAM

Draw RAM and ROM for the truth table given below.